DECLARATION

I, the undersigned, of 15-29, Tsukamoto, 3-chome, Yodogawa-ku, Osaka 532-0026, JAPAN, hereby certify that I am well acquainted with the English and Japanese languages, that I am an experienced translator for patent matter, and that the attached document is a true English translation of

Japanese Patent Application No. 2004-079873.

I declare that all statements made herein of my own knowledge are true, that all statements on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Signature:

Natsuko Honjo

Dated: September 16, 2008

[Title of the Invention] Gallium Nitride Based Compound Semiconductor Light Emitting Device

[Claims]

[Claim 1] A gallium nitride based compound semiconductor light emitting device comprising; a substrate made of a gallium nitride based compound semiconductor; a first n-type layer containing at least In; and a light emitting layer, wherein the first n-type layer is formed between the substrate and the light emitting layer.

[Claim 2] A gallium nitride based compound semiconductor light emitting device according to claim 1, wherein the gallium nitride based compound semiconductor is GaN.

[Claims 3] A gallium nitride based compound semiconductor light emitting device according to claim 1 or 2, wherein the substrate is polished.

[Claim 4] A gallium nitride based compound semiconductor light emitting device according to claim 3, wherein the polished substrate is etched.

[Claim 5] A gallium nitride based compound semiconductor light emitting device according to claim 4, wherein the surface of the substrate is flat.

[Claim 6] A gallium nitride based compound semiconductor light emitting device according to any one of claims 1 to 5, wherein a second n-type layer made of a gallium nitride based compound semiconductor is formed between the substrate and the first n-type layer.

[Claim 7] A gallium nitride based compound semiconductor light emitting device according to any one of claims 1 to 6, wherein a third n-type layer made of a gallium nitride based compound semiconductor is formed between the first n-type layer and the light emitting layer.

[Claim 8] A gallium nitride based compound semiconductor light emitting device according to claim 7, wherein the third n-type layer is a cladding layer.

[Claim 9] A gallium nitride based compound semiconductor light emitting device

according to claim 8, wherein the n-type cladding layer contains at least AlGaN or GaN.

[Claim 10] A gallium nitride based compound semiconductor light emitting device according to any one of claims 1 to 9, wherein the first n-type layer has a thickness in a range between 10 nm and 1 μm.

[Claim 11] A gallium nitride based compound semiconductor light emitting device according to any one of claims 1 to 9, wherein the first n-type layer is InAlGaN or InGaN.

[Detailed Description of the Invention]

[Technical Field]

The present invention relates to gallium nitride based compound semiconductor light emitting devices utilized in optical devices, such as a light emitting diode, a laser diode, and the like.

[Background of the Invention]

Recently, gallium nitride based compound semiconductors are used as semiconductor materials for light emitting devices operated in a waveband ranging from visible light to ultraviolet light and high power output electronic devices operated at high temperature (Patent Document 1, for example). As a substrate used for a nitride semiconductor light emitting device, conductive substrates, such as a GaN substrate has been used in place of an insulating substrate, such as a sapphire substrate. The use of a conductive substrate allows the current to flow in the substrate to reduce the resistance of current paths. This reduces power consumption and the operation voltage and increases the electrostatic withstanding voltage.

A conventional gallium nitride based compound semiconductor is shown in FIG. 1. In FIG. 1, an n-type layer 2 made of GaN, a light emitting layer 5 made of InGAN, and a p-type layer 6 made of AlGaN are layered in this order on an n-type substrate 1 made of GaN. A p-side electrode 7 is formed on the surface of the p-type layer 6, and an n-side electrode 8 is formed on the surface of the n-type layer 2 which is exposed by removing by

etching each part of the p-type layer 6, the light emitting layer 5, and the n-type layer 2 from the surface side of the p-type layer 6 (Patent Document 2, for example).

[Patent Document 1] Japanese Unexamined Patent Application Publication 2001-60719

[Patent Document 2] Japanese Unexamined Patent Application Publication 2001-345476

[Summary of the Invention]

[Problems that the Invention is to Solve]

The use of a GaN substrate as a substrate, however, necessitates polishing for flattening the surface of the GaN substrate to invite physical damages to the surface of the GaN substrate, thereby causing non-uniform light emission from the light emitting layer formed thereon.

The present invention has been made in view of the foregoing and has its object of improving the uniformity of light emission.

[Means for Solving the Problems]

To attain the above object, the present invention is composed of a substrate made of a gallium nitride based compound semiconductor, a first n-type layer containing at least In, and a light emitting layer, wherein the first n-type layer is formed between the substrate and the light emitting layer. The first n-type layer containing at least In relaxes non-uniform strain of the crystals and damages that the substrate, which is made of a gallium nitride based compound semiconductor and which has a polished surface to be flattened, involves.

Formation of a second n-type layer made of a gallium nitride based compound semiconductor between the substrate and the first n-type layer buries microscopic roughness that the gallium nitride based compound semiconductor substrate has. Further, the distance from the substrate to the light emitting layer can be set large to less involve interface influence, such as contamination by an impurity on the surface of the substrate. Moreover, by growing on the substrate the second n-type layer having substantially the

same lattice constant as that of the substrate, the second n-type layer can be formed with no additional strain caused to attain stable formation of the first n-type layer grown on the second n-type layer. Furthermore, when the layer containing In is formed thick for setting the distance from the substrate to the light emitting layer large, a crack is formed. However, the second n-type layer grown thick prevents such a crack from being formed.

Formation of a third n-type layer made of a gallium nitride based compound semiconductor between the first n-type layer and the light emitting layer sets the distance from the substrate to the light emitting large to less involve interface influence, such as contamination by an impurity and the like on the surface of the substrate. Further, when the layer containing In is formed thick for setting the distance from the substrate to the light emitting layer large, a crack is formed. However, the third n-type layer grown thick prevents such a crack from being formed.

[Effects of the Invention]

In the gallium nitride based compound semiconductor light emitting device of the present invention, the first n-type layer containing at least In relaxes non-uniform strain and damages that the gallium nitride based compound semiconductor substrate involves to improve the in-plane uniformity of the wafer as a light emitting characteristic and the yields.

[Best Mode for Carrying out the Invention]

An embodiment of the present invention will be described below with reference to the accompanying drawings.

In FIG. 2, there are stacked in this order on a substrate 11 made of a gallium nitride based compound semiconductor a second n-type layer 12 made of a gallium nitride based semiconductor, a first n-type layer 13 containing at least In, a cladding layer 14, a light emitting layer 15, and a p-type layer 16. A p-side electrode 17 is formed on the surface of the p-type layer 16, and an n-side electrode 18 is formed on the surface of the second

n-type layer 12 which is exposed by removing by etching from the surface side of the p-type layer 16 each part of the p-type layer 16, the light emitting layer 15, the cladding layer 14, the first n-type layer 13, and the second n-type layer 12.

As the substrate 11, an n-type gallium nitride based compound semiconductor ($In_aAl_bGa_{1-a-b}N$, wherein $0\leq a\leq 1$, $0\leq b\leq 1$, and $0\leq a+b\leq 1$) can be used, wherein $Al_cGa_{1-c}N$ (wherein $0\leq c\leq 1$) from which excellent crystallinity can be easily obtained is desirable. Among of all, the use of a substrate made of GaN, which is comparatively easy to manufacture and from which the most excellent crystallinity can be obtained, is preferable. An n-type impurity, such as Si, Ge, or the like may not be doped in the substrate 11, but such doping reduces the device resistance. In doping, the electron density is controlled to be in the range between $1x10^{17}$ cm^{-3} and $1x10^{20}$ cm^{-3}. The electron density of lower than $1x10^{17}$ cm^{-3} increases the resistivity to invite a tendency of inhibiting the electrons doped to the substrate 11 from diffusing in the substrate 11. While, the electron density of higher than $1x10^{20}$ cm^{-3} invites a tendency of worsening the crystallinity of the substrate 11, which is caused due to high density doping of the n-type impurity.

As the second n-type layer 12, an n-type gallium nitride based compound semiconductor having substantially the same lattice constant as that of the substrate can be used. This permits microscopic roughness that the gallium nitride based semiconductor substrate involves to be buried. Further, this increases the distance from the substrate 11 to the light emitting layer 15 to less invite interface influence, such as contamination by an impurity on the surface of the substrate 11. Since the second n-type layer 12 having substantially the same lattice constant as that of the substrate 11 is grown on the substrate 11, the second n-type layer 12 can be formed without causing new strain, which leads to stable formation of the first n-type layer 13 grown on the second n-type layer 12. When the layer containing In is formed thick for increasing the distance between the substrate 11 and the light emitting layer 15, a crack is formed. However, when the second n-type layer 12 is grown thick, such a crack can be prevented from being formed. As the second

n-type layer 12, a single layer of GaN, AlGaN, InGaN, In AlGaN, or the like or a stacked layer thereof can be used. Though the second n-type layer 12 is preferably made of an n-type gallium nitride based compound semiconductor having substantially the same lattice constant as that of the substrate, InGaN or InAlGaN having a small composition ratio of In may be used because their lattice constants are close to the lattice constant of the substrate.

In at least a layer of the second n-type layer 12 on which the n-side electrode 18 is formed, it is preferable that an n-type impurity, such as Si, Ge, or the like is doped and the electron density thereof is set in the range between $1x10^{17}$ cm^{-3} inclusive and $1x10^{20}$ cm^{-3} exclusive. The electron density lower than $1x10^{17}$ cm^{-3} increases the ohmic contact resistance with the n-side electrode 18 to increase the operation voltage of the light emitting device. While, the electron density higher than $1x10^{20}$ cm^{-3} invites a tendency of worsening the crystallinity of the second n-type layer 12 which is cased due to high density doping of the n-type impurity.

The second n-type layer 12 preferably has a thickness of 100 nm or larger. The second n-type layer 12 thinner than 100 nm invites much difficulty in attaining etching accuracy in forming the exposed face of the second n-type layer 12 by etching for forming the n-side electrode 18. Though there is no specific upper limit of the thickness of the second n-type layer 12, it is preferable to set it at about 5 μm or smaller for relaxing the etching accuracy in forming the exposed face and for preventing unnecessary prolongation of the time required for forming the second n-type layer 12.

As the first n-type layer 13 containing at least In, there may be used a single layer of InGaN, InAlGaN, or InAlN, a multilayered film layer including at least one of the single layers containing In, or a multilayered film layer obtained by alternatively stacking one of the layers containing In and a layer not containing In, such as GaN, AlGaN. A semiconductor layer containing In is comparatively soft, and accordingly, non-uniform strain caused due to damages of the substrate can be relaxed. Although InGaN that can easily manufactured is preferable among of all, the contained Al increases the band gap to

allow the light emitted from the light emitting layer 15 to be less absorbed. Therefore, InAlGaN may be used for the light in the light emitting range from blue to ultraviolet. At least In is contained in the first n-type layer 13, of which composition ratio is preferably in the range between 0.01 and 0.10. In larger than 0.01 enhances the effect of being soft further to absorb non-uniform strain caused due to damages of the substrate. In smaller than 0.10 minimizes compression strain caused in the first n-type layer 13 itself, which is due to an increase in the composition ratio of In, and accordingly, no defects is caused in the layer itself. This involves no worsening of the crystallinity. Further, the composition ratio of In between 0.02 and 0.07 is especially preferable because the aforementioned effects can be obtained remarkably. The thickness of the first n-type layer 13 is preferably in the range between 10 nm and 1 μm. The first n-type layer 13 having a thickness of larger than 10 nm stably attains the effect of uniforming the light emitting characteristics within the wafer plane. The first n-type layer 13 having a thickness of smaller than 1 μm can prevent degradation of the crystallinity of the n-type first layer and contemplate shortening of the time required for manufacturing the fist n-type layer 13. Particularly, it is preferable to set it in the range between 20 nm and 100 nm. The first n-type layer 13 having an thickness larger than 20 nm can stably attain uniformity of the light emitting characteristics within the wafer plane. The first n-type layer 13 having a thickness of smaller than 100 nm can further prevent degradation of the crystallinity of the first n-type layer and contemplate shortening of the time required for manufacturing the first n-type layer 13. The first n-type layer 13 may be a non-doped layer, but preferably, an n-type impurity is doped. Particularly, Si or Ge is preferable. Electrons are excellently diffused within the plane. The first n-type layer is preferably a layer to which an n-type impurity, such as Si, Ge, or the like is doped and which has an electron density in the range between $1x10^{17}$ cm^{-3} inclusive and $1x10^{20}$ cm^{-3} exclusive.

As the cladding layer 14, GaN or AlGaN can be used. When the cladding layer 14 is made of a gallium nitride based compound semiconductor having a band gap larger

than that of the first n-type layer, hole overflow from the light emitting layer can be suppressed effectively. An n-type impurity may be or may not be doped in the cladding layer 14. The cladding layer 14 preferably has a carrier density smaller than the second or first n-type layer. With this arrangement, the electrons in the n-type layers hardly flow toward the light emitting layer 15 temporarily to diffuse uniformly in the plane of the n-type layers, resulting in realization of uniform electron implantation to the light emitting layer 15. This uniforms the light emitting distribution in the light emitting layer 15 to attain uniform surface emission by the principal light emitting face on the reverse side of the substrate 11. The thickness of the cladding layer 14 is preferably set within the range between 10 nm and 200 nm, both inclusive. The cladding layer thinner than 10 nm invites a tendency of reducing the effect of current spreading while that thicker than 200 nm increases the series resistance of the light emitting device to increase the operation voltage.

The light emitting layer 15 may be made of a gallium nitride based compound semiconductor having a band gap smaller than the band gaps of the second n-type layer 12 and the p-type layer 16. Particularly, the use of InGaN or GaN not containing Al enhances the light emitting strength in the wavelength range from ultraviolet to green. In the case of the light emitting layer 15 containing In, when the light emitting layer 15 has a film thickness of 10 nm or smaller and is formed of a single quantum well layer, the crystallinity of the light emitting layer 15 is enhanced and the light emitting efficiency increases further.

The light emitting layer 15 may have a multi-quantum well structure in which a quantum well layer made of InGaN or GaN and a barrier layer made of InGaN, GaN, AlGaN, or the like and having a band gap larger than that of the quantum well layer are stacked alternately.

The p-type layer 16 may be made of a p-type gallium nitride based compound semiconductor having a band gap larger than that of the light emitting layer 15. This

provides a function as a p-type cladding layer to the p-type layer 16. The p-type layer 16 may be a single layer of GaN, AlGaN, InGaN, InAlGaN or the like or a multilayer thereof. Particularly, the use of AlGaN as the p-type layer in contact with the light emitting layer 15 attains efficient confinement of the electrons within the light emitting layer 15 to increase the light emitting efficiency.

The p-type layer 16 is doped with a p-type impurity to be p-type conductive. The p-type impurity may be Mg, Zn, Cd, C, or the like, wherein Mg is preferable because it can set a layer to be p-type comparatively easily. The p-type impurity density is preferably set in the range between $1x10^{19}$ cm^{-3} inclusive and $5x10^{20}$ cm^{-3} exclusive. The p-type impurity density of lower than $1x10^{19}$ cm^{-3} increases the ohmic contact resistance with the p-side electrode 17 to increase the operation voltage of the light emitting device. The p-type impurity density of higher than $5x10^{20}$ cm^{-3} involves a tendency of worsening the crystallinity of the p-type layer 16 which is caused due to high density doping of the p-type impurity and involves remarkable diffusion of the p-type impurity to the light emitting layer 15, thereby lowering the light emitting efficiency.

In the case where a p-type impurity is doped at a comparatively high density to the p-type layer 16, an intermediate layer may be introduced between the light emitting layer 15 and the p-type layer 16 for suppressing excessive diffusion of the p-type impurity to the light emitting layer 15. The intermediate layer may be made of InAlGaN, but the use of GaN or AlGaN is especially preferable because the crystallinity at the interface with the light emitting layer 15 can be kept excellently. The intermediate layer, which plays a role of a layer for absorbing the p-type impurity diffusing toward the light emitting layer 15, is preferably undoped. The thickness of the intermediate layer is preferably in the range between 1 nm and 50 nm, both inclusive. The intermediate layer having a thickness of smaller than 1 nm minimizes the effect of suppressing diffusion of the p-type impurity toward the light emitting layer 15 while that having a thickness of larger than 50 nm lowers the hole implantation efficiency to the light emitting layer 15 to lower the light emitting

efficiency.

The layer thickness of the p-type layer 16 is preferably in the range between 50 nm and 500 nm, both inclusive. When the p-type layer 16 is thinner than 50 nm, the meal composing the p-side electrode 17 invades the light emitting layer 15 by electro-migration and the like to shorten the lifetime of the light emitting device. While, when the p-type layer 16 is thicker than 500 nm, voltage drop increases when the current (hole) passes through the p-type layer 16 to increase the operation voltage of the light emitting device.

The side of the p-type layer 16 which is in contact with the p-side electrode 17 may be made of GaN or InGaN having a comparatively small band gap. This minimizes the contact resistance with the p-side electrode 17 to reduce the operation voltage effectively.

The p-side electrode 17 may made of a single metal, such as Au, Ni, Pt, Pd, Mg, or the like, an alloy thereof, or a layered structure thereof. Particularly, the use of metal having a high reflectivity with respect to a light emitting wavelength, such as Ag, Pt, Mg, Al, Zn, Rh, Ru, Pd, or the like allows the light from the light emitting layer 15 toward the p-side electrode 17 to be reflected to take it out from the reverse face of the substrate 11. Hence, it is preferable in the aspect of enhancing the light emitting strength.

The n-side electrode 18 is formed in contact with the surface of the second n-type layer 12 which is exposed by removing a part of a layered structure of the first n-type layer 13, the cladding layer 14, the light emitting layer 15, and the p-type layer 16 formed on the second n-type layer 12 from the surface side of the layered structure. This arrangement of the n-side electrode 18 allows the reverse face of the substrate 11 not in the aforementioned layered structure to be a principal light emitting face, thereby obtaining uniform face emitting light in the principal light emitting face.

The n-side electrode 18 may be made of a single metal of Al, Ti, or the like, an alloy containing Al, Ti, Au, Ni, V, Cr, or the like, or a layered structure thereof.

In the case where the electron carrier density of the substrate 11 is equal to or

higher than that of the second n-type layer 12, the n-side electrode 18 may be formed in contact with the surface of the substrate 11 which is exposed by removing a part of the layered structure of the first n-type layer 13, the cladding layer 14, the light emitting layer 15, and the p-type layer 16 formed on the second n-type layer 12 from the surface thereof. Provision of the n-side electrode 18 on the substrate 11 having a high electron carrier density reduces the ohmic contact resistance of the n-side electrode 18 to lower the operation voltage.

Alternatively, the n-side electrode 18 may be formed in contact with the surface of the substrate 11 which is opposite to the light emitting layer 15. This arrangement of the n-side electrode 18 eliminates the need to save a space for forming the n-side electrode to minimize the chip size.

Alternatively, the n-side electrode 18 may be formed in contact with the surface of the first n-type layer 13 which is exposed by removing a part of the layered structure of the cladding layer 14, the light emitting layer 15, and the p-type layer 16 formed on the first n-type layer 13 from the surface side thereof. The formation of the n-side electrode 18 on the first n-type layer 13 having a small band gap reduces the ohmic contact resistance of the n-side electrode 18.

Further, a p-type cladding layer (not shown) may be formed between the light emitting layer 15 and the p-type layer 16. Preferably, the p-type cladding layer is made of a gallium nitride based compound semiconductor having a band gap larger than that of the light emitting layer 15 and is especially preferably made of $Al_uGa_{1-u}N$ (wherein $0 \leq u < 1$) to which a p-type impurity, such as Mg or the like is doped. In general, a p-type cladding layer is formed at a growth temperature higher than a temperature suitable for growing the light emitting layer 15 for forming crystals excellently in many cases, and therefore, the crystallinity of the light emitting layer 15 may be degraded by dissociation or the like of the elements, such as indium, nitrogen, and the like composing the light emitting layer 15 in the time until temperature rise up to the growth temperature of the p-type cladding layer

after growth of the light emitting layer 15. In view of this, a part of the p-type cladding layer which is in contact with the light emitting layer 15 is grown and formed continuously with the temperature raised after growth of the light emitting layer 15, and the remaining part of p-type cladding layer is grown subsequently at the growth temperature of the p-type cladding layer. This attains effective prevention of degradation of the crystallinity of the light emitting layer 15. At this time, the part of the p-type cladding layer which is grown with temperature raised is preferably made of $Al_vGa_{1-v}N$ (wherein $0 \leq v < 1$ and $v \leq u$). Because, it can exhibit fully the function as a cladding layer formed in contact with the light emitting layer 15, and the effect of preventing degradation of the crystallinity, which is caused due to dissociation or the like of the elements composing the light emitting layer 15 can be enhanced.

Furthermore, as shown in FIG. 3, the n-type layer may have a layered structure including from the substrate 11 side a fourth n-type layer 31 having a low carrier density and a fifth n-type layer 32 having a high carrier density. In other words, this n-type layer is formed by forming the fourth n-type layer 31 having a low carrier density on the substrate 11 side and then forming the fifth n-type layer 32 having a high carrier density on the fourth n-type layer 31, and then, the n-side electrode 18 is formed on the fifth n-type layer 32.

With the layered structure in which the fourth n-type layer 31 and the fifth n-type layer 32, of which carrier densities are different from each other, are formed in this order from the substrate 11 side, the fourth n-type layer 31 can be thick even if the carrier density of the fourth n-type layer 31 is set small by reducing the doping amount of the n-type impurity to the fourth n-type layer 31. This suppresses both an increase in resistance of the fourth n-type layer 31 and formation of a crack. When the n-side electrode 18 is formed on the fifth n-type layer 32 having a high carrier density by increasing the doping amount of the n-type impurity larger than that in the fourth n-type layer 31 and formed on the fourth n-type layer 31, the contact resistance between the fifth n-type layer 32 and the

n-side electrode 18 can be reduced to lower the operation voltage of the light emitting device, thereby enabling reduction in power consumption.

As described above, the difference in carrier density between the fourth and fifth n-type layers 31, 32 promotes optimization of operation voltage lowering and prevention of crack formation. Specification of concrete numerical values of the respective carrier densities are as follows according to the acknowledgement of the inventors.

First, the carrier density of the fourth n-type layer 31 is preferably in the range between $1x10^{17}$ cm^{-3} and $2x10^{18}$ cm^{-3}. The carrier density of the fourth n-type layer 31 lower than $1x10^{17}$ cm^{-3} involves a tendency of increasing the series resistance of the fourth n-type layer 31 itself to increase the operation voltage of the device. While, the carrier density thereof higher than $2x10^{18}$ cm^{-3} involves a tendency of inviting crack formation.

The carrier density of the fifth n-type layer, which is higher than that of the fourth n-type layer 31, is preferably set in the range between $2x10^{18}$ cm^{-3} and $1x10^{19}$ cm^{-3}. The carrier density of the fifth n-type layer 32 lower than $2x10^{18}$ cm^{-3} involves difficulty in sufficient reduction in contact resistance with the n-side electrode 18. The carrier density thereof higher than $1x10^{19}$ cm^{-3} involves a tendency of worsening the crystallinity of this layer to worsen the crystallinity of the light emitting layer and the p-type layer grown thereon, thereby inviting lowering of the light emitting output.

Further, it is preferable to set the thickness of the fifth n-type layer 32 to be smaller than that of the fourth n-type layer 31 and especially to set it in the range between 100 and 500 nm. The fifth n-type layer 32 thinner than 100 nm involves difficulty in controlling the etching depth in exposing the surface of the n-type layer by removing each part of the p-type layer 16, the light emitting layer 15, the cladding layer 14, the first n-type layer 13, and the fifth n-type layer 32. The fifth-type layer 32 thicker than 500 nm worsens the crystallinity of the fifth n-type layer 32 to worsen the crystallinity of the first n-type layer 13, the cladding layer 14, the light emitting layer 15, and the p-type layer 16 grown on the fifth n-type layer 32, thereby inviting lowering of the light emitting output.

The layer thickness of the fourth n-type layer 31 is preferably set in the range between 1 and 5 μm. The thickness thinner than 1 μm involves a tendency of increasing the series resistance of the device to increase the operation voltage while the thickness thereof thicker than 5 μm invites crack formation. As described above, a structure may be employed in which the fourth n-type layer 31 and the fifth n-type layer 32 are formed between the substrate 11 and the first n-type layer 13 and a layered structure including an n-type layer having a low carrier density and an n-type layer having a high carrier density is formed between the first n-type layer 13 and the light emitting layer 15. Further, though not shown, only a layered structure including an n-type layer having a low carrier density and an n-type layer having a high carrier density may be formed only between the first n-type layer 13 and the light emitting layer 15.

(Embodiment 1)

Embodiment 1 of the present invention will be described next. The difference of Embodiment 1 from the above described best mode for carrying out the invention lies in that a third n-type layer made of a gallium nitride based compound semiconductor is formed on a layer containing at least In. Specifically, the layer containing at least In is interposed between n-type layers made of a gallium nitride based compound semiconductor. The other aspects are basically the same as those in the best mode for carrying out the invention, unless otherwise described.

An n-type impurity, such as Si, Ge, or the like is doped in a third n-type layer 19 shown in FIG. 4, and its electron density is preferably set in the range between $1x10^{17}$ cm^{-3} and $1x10^{20}$ cm^{-3}. The electron density of lower than $x10^{17}$ cm^{-3} increases the ohmic contact resistance with the n-side electrode 18 to increase the operation voltage of the light emitting device while that of higher than $1x110^{20}$ cm^{-3} invites a tendency of worsening the crystallinity of the second n-type layer 12 which is caused due to high density doping of the n-type impurity.

The third n-type layer 19 is preferable set to have a thickness of equal to or larger

than 100 nm. The thickness thinner than 100 nm involves much difficulty in attaining etching accuracy in forming the exposed face for forming the n-side electrode 18 in the third n-type layer 19 by etching the third n-type layer 19. Though there is no specific upper limit of the thickness of the third n-type layer 19, it is preferable to set it to be equal to or smaller than 5 μm for relaxing the etching accuracy in forming the exposed face and for preventing time required for forming the third n-type layer 19 from being unnecessarily prolonged. The n-side electrode 18 is formed on the third n-type layer 19.

[Working Examples]

Specific examples of a method of manufacturing a gallium nitride based compound semiconductor light emitting device of the present embodiment will be described with reference to the drawings. The following working examples show a method of growing a gallium nitride based compound semiconductor mainly using an organic metal vapor phase epitaxy method, but the growth method is not limited thereto and may employ a molecular beam epitaxy method, an organic metal molecular beam epitaxy method, or the like.

(Working Example 1)

FIG. 2 is a sectional view showing a structure of a gallium nitride based compound semiconductor light emitting device according to another embodiment of the present invention.

In the present working example, the gallium nitride based compound semiconductor light emitting device shown in FIG. 2 was manufactured.

First, a GaN single crystal film grown to have a thickness of approximately 370 μm on the surface of a sapphire substrate by halide vapor growth was removed from the sapphire substrate by irradiating YAG laser light having a wavelength of 355 nm from the reverse face of the sapphire substrate. Then, a disc was attached thereto with the face from which the GaN single crystal film has been removed facing downward, and the surface was flattened and mirror-polished by abrasive grains including diamond particles with the use of a polishing apparatus. Thereafter, the GaN single crystal film was

removed from the disc and was cleaned with an organic solvent and an acid solution. Thus, a GaN substrate 11 made of GaN single crystal film having a thickness of approximately 350 μm and a diameter of approximately 50 mm was obtained.

Next, after the substrate 11 was placed on a substrate holder in a reaction tube and was kept at a temperature at 1060 °C for 10 minutes, then cleaning was performed for removing contamination, such as an organic matter and the like and moisture adhering to the surface of the substrate 11 by heating the substrate 11 with a hydrogen gas, a nitrogen gas, and ammonium allowed to flow at 7 litter per minutes, 7 litter per minute, and 6 litter per minute, respectively.

Subsequently, while the temperature of the substrate 11 was kept at 1060 °C, ammonium of 6 litter per minutes, trimethyl gallium (hereinafter abbreviated it as TMG) of 80 μ mol per minute, and 10 ppm-diluted mono-silane of 30 cc per minute were supplied with a nitrogen gas of 7 litter per minute and a hydrogen gas of 7 litter per minute allowed to flow as a carrier gas, thereby growing the second n-type layer 12 made of GaN to which Si is doped and having a thickness of 2 μm. The electron density of the second n-type layer 12 was $3x10^{18}$ cm^{-3}.

Following the growth of the second n-type layer 12, supply of TMG and mono-silane was stopped, and the temperature of the substrate 11 was lowered to 760 °C. Then, ammonium of 6 litter per minute, TMG of 12 μ mol per minute, trimethyl indium (hereinafter abbreviated it as TMI) of 1 μ mol per minute, and mono-silane of 1.5 cc per minute were supplied with the temperature kept and with a nitrogen gas of 14 litter per minute allowed to flow as a carrier gas, thereby growing the first n-type layer 13 made of $In_{0.05}Ga_{0.95}N$ to which Si is doped and having a thickness of 50 nm. The electron density of the first n-type layer 13 was $1x10^{18}$ cm^{-3}.

After the first n-type layer 13 was grown, supply of TMI was stopped, and a nitrogen gas of 14 litter per minute, ammonium of 6 litter per minute, and TMG of 2 μ mol per minute was supplied as a carrier gas with the temperature of the substrate 1 raised up to

1060 °C, thereby subsequently growing undoped GaN (not shown) to have a thickness of 3 nm. When the temperature of the substrate 11 reached 1060 °C, ammonium of 4 litter per minute, TMG of 40 μ mol per minute, and trimethyl aluminum (hereinafter abbreviated it as TMA) of 3 μ mol per minute were supplied with a nitrogen gas of 8 litter per minute and a hydrogen gas of 8 litter per minute allowed to flow as a carrier gas, thereby growing the undoped cladding layer 14 made of $Al_{0.05}Ga_{0.95}N$ and having a thickness of 30 nm. The electron density of the cladding layer 14 was $5x10^{16}$ cm^{-3}.

Following the growth of the cladding layer 14, supply of TMG and TMA was stopped, and the temperature of the substrate 11 was lowered up to 700 °C. Then, a nitrogen gas of 12 litter per minute, ammonium of 8 litter per minute, TMG of 4 μ mol per minute, and TMI of 5 μ mol per minute were supplied as a carrier gas with the temperature of the substrate kept at that temperature, thereby growing an undoped well layer (not shown) having a quantum well structure made of $In_{0.15}Ga_{0.85}N$ and having a thickness of 2 nm.

After the formation of the well layer, supply of TMI was stopped. A nitrogen gas of 12 litter per minute, ammonium of 8 litter per minute, and TMG of 2 μ mol per minute were supplied as a carrier gas with the temperature of the substrate 1 raised up to 1060 °C to grow subsequently an undoped GaN barrier layer (not shown) having a thickness of 3 nm. When the temperature of the substrate 11 reached 1060 °C, ammonium of 6 litter per minute and TMG of 40 μ mol per minute were supplied with a nitrogen of 7 litter per minute and hydrogen of 7 litter per minute allowed to flow as a carrier gas to grow subsequently an undoped GaN barrier layer (not shown) having a thickness of 12 nm. Thus, an undoped barrier layer made of GaN and having a thickness of 15 nm was formed. Then, supply of TMG was stopped, and the temperature of the substrate is lowered again to 700 °C. This formation method of the well layer (not shown) and the barrier layer (not shown) was repeated to thus form a well layer (not shown), a barrier layer (not shown), a well layer (not shown), a barrier layer (not shown), and a well layer (not shown).

After the formation of the last well layer (not sown), supply of TMI was stopped. Then, nitrogen of 14 litter per minute, ammonium of 6 litter per minute, TMG of 2 μ mol per minute, and TMA of 0.15 μ mol per minute were supplied as a carrier gas with the temperature of the substrate 11 raised up to 1060 °C to grow subsequently an undoped $Al_{0.05}Ga_{0.95}N$ (not shown) having a thickness of 3 nm.

In this way, a MQW formed of four well layers was formed.

Thereafter, after the substrate temperature reached 1060 °C, ammonium of 4 litter per minute, TMG of 40 μ mol per minute, TMA of 3 μ mol per minute, and bis(cyclopentadienyl)magnesium (hereinafter abbreviated it as Cp_2Mg) of 0.1 μ mol per minute were supplied with a nitrogen gas of 10 litter per minute and a hydrogen gas of 6 litter per minute allowed to flow as a carrier gas, thereby growing an Mg-doped p-type layer 16 made of $Al_{0.05}Ga_{0.95}N$ and having a thickness of 200 nm. The Mg density of the thus grown p-type layer 16 was $1x10^{20}$ cm^{-3}.

After the growth of the p-type layer 16, supply of TMG, TMA, and Cp_2Mg was stopped. Then, the substrate 11 was cooled to approximately the room temperature with a nitrogen gas of 18 litter per minute and ammonium of 2 litter per minute allowed to flow. Then, a wafer having the substrate 11 on which the gallium nitride based compound semiconductors are layered was taken out from the reaction tube.

The in-plane distribution of the photo luminescence intensity of the wafer was measured at 1 mm pitch by a photoluminescence mapping apparatus using He-Cd laser light having a wavelength of 325 nm as an excitation light source to find that the standard deviation in the wafer having a diameter of 50 nm was 4.1 %.

On the surface of the layered structure made of the thus formed gallium nitride based compound semiconductors, an SiO_2 film was deposited by CVD without performing additional annealing. Then, patterning in substantially square shape was performed by photolithography and wet etching to form an SiO_2 mask for etching. Then, each part of the p-type layer 16, the light emitting layer 15, the cladding layer 14, the first n-type layer

13, and the second n-type layer 12 were removed in the direction reverse to the stacking direction by approximately 500 nm depth by reactive ion etching to expose the surface of the second n-type layer 12. The n-side electrode 18 in which Ti of 100 nm thickness and Au of 500 nm thickness are layered was deposited and formed on a part of the exposed surface of the second n-type layer 12 by photolithography and vapor deposition. Further, after the SiO2 mask for etching was removed by wet etching, the p-side electrode 17 of Pt of 5 nm, Rh of 500 nm, Ti of 100 nm, and Au of 500 nm are deposited and formed on the entirety of the surface of the p-type layer 16 by photolithography and vapor deposition.

Next, the reverse face of the substrate 11 was polished to adjust the thickness to be approximately 100 μm, and the wafer was separated into chips by scribing. In this way, the gallium nitride based compound semiconductor light emitting device shown in FIG. 2 was obtained.

This light emitting device was bonded with its electrode formation face facing downward by means of an Au bump on an Si Zener diode including a pair of positive and negative electrodes. In so doing, the light emitting device was boarded so that the p-side electrode 17 and the n-side electrode 18 of the light emitting device are connected the negative electrode and the positive electrode of the Si Zener diode, respectively. Thereafter, the Si Zener diode on which the light emitting device is boarded was placed on a stem by means of an Ag paste, the positive electrode of the Si Zener diode was connected to the electrode on the step by means of a wire, and then, resin molding was performed to thus manufacture a light emitting diode. When the thus manufactured light emitting diode was driven by a forward current at 20 mA, a blue light having a peak light emitting wavelength of approximately 470 nm was emitted and uniform surface emitting light was obtained from the reverse side of the substrate 11. The light emitting output at that time was small in variation among individual light emitting diodes and was approximately 6 mW. The forward operation voltage was approximately 3.0 V.

(Working example 2)

In Working Example 2, a light emitting diode was manufactured by the same manner as in Working Example 1 except that the surface of the GaN substrate 11 was etched by reactive ion etching before growing the second n-type layer 12 in Working Example 1.

Specifically, after the GaN substrate 11 was prepared of which surface has been flattened and mirror-polished by the same manner as in Working Example 1, the GaN substrate 11 was set in a reactive ion etching apparatus, and the surface of the GaN substrate 11 was etched by approximately 100 nm in thickness with a chlorine gas allowed to flow at 10 sccm as a process gas, the high frequency power set at 100 W, and the substrate temperature set at 50 °C.

Next, the second n-type layer 12, the first n-type layer 13, the cladding layer 14, the light emitting layer 15, and the p-type layer 16 were grown sequentially on the surface of the GaN substrate 11 by the same manner as in Working Example 1 to form a wafer having the substrate 11 on which the gallium nitride based compound semiconductors are stacked.

Subsequently, the in-plane distribution of the photoluminescence strength of the wafer was measured by the same manner as in Working Example 1 to find that the standard deviation in the wafer of 50 mm diameter was 3.0 %.

Electrodes are formed on the layered structure of the thus formed gallium nitride based compound semiconductors by the same manner as in Working Example 1, and packaging was performed to manufacture a light emitting diode. When the thus manufactured light emitting diode was driven by a forward current at 20 mA, blue light having a peak light emitting wavelength of approximately 470 nm was emitted and uniform surface emitting light was obtained from the reverse side of the substrate 11. The light emitting output at that time was small in variation among individual light emitting diodes and was approximately 6 mW. The forward operation voltage was approximately 3.0 V.

(Comparative Example)

In Comparative Example, a light emitting diode was manufactured by the same manner as in Working Example 1 except that the first n-type layer 13 is not formed in Working Example 1.

Specifically, in Working Example 1, after the second n-type layer 12 was grown, an undoped cladding layer 14 made of $Al_{0.05}Ga_{0.95}N$ was grown by the same manner as in Working Example 1 with the temperature of the substrate 11 kept at 1060 °C, and then, the light emitting layer 15 and the p-type layer 16 were grown sequentially to form a wafer including the substrate 11 on which the gallium nitride based compound semiconductors are stacked.

Next, the in-plane distribution of the photoluminescence strength of the wafer was measured by the same manner as in Working Example 1 to find that the standard deviation in the wafer of 50 mm diameter was 32.9 %.

Electrodes are formed on the layered structure of the thus formed gallium nitride based compound semiconductors by the same manner as in Working Example 1, and packaging was performed to manufacture a light emitting diode. When the thus manufactured light emitting diode was driven by a forward current at 20 mA, blue light having a peak light emitting wavelength of approximately 470 nm was emitted. The light emitting output at that time was large in variation among individual light emitting diodes and ranges from 3 mW to 6 mW. The forward operation voltage varies in the range between 3.0 V and 3.3 V.

[Industrial Applicability]

In the present invention, the first n-type layer containing at least In relaxes non-uniform strain and damages that the GaN substrate involves to exhibit an effect of improving uniformity in wafer plane as a light emitting characteristic and the yields, and accordingly, a light emitting diode and a laser diode can be realized at low manufacturing cost.

[Brief Description of the Drawings]

[FIG. 1] FIG. 1 is a sectional view showing a structure of a conventional gallium nitride based compound semiconductor device.

[FIG. 2] FIG. 2 is a sectional view showing a structure of a gallium nitride based compound semiconductor device according to the best mode for carrying out the present invention.

[FIG. 3] FIG. 3 is a sectional view showing a structure of a gallium nitride based compound semiconductor device according to the best mode for carrying out the present invention.

[FIG. 4] FIG. 4 is a sectional view showing a structure of a gallium nitride based compound semiconductor device according to Embodiment 1 of the present invention.

[Index of Reference Numerals]

1	n-type substrate made of GaN
2	n-type layer made of GaN
5	light emitting layer made of InGaN
6	p-type layer made of AlGaN
7	p-side electrode
8	n-side electrode
11	substrate
12	second n-type layer
13	first n-type layer
14	cladding layer
15	light emitting layer
16	p-type layer
17	p-side electrode

18 n-side electrode

19 third n-type layer

31 fourth n-type layer

32 fifth n-type layer

[Abstract]

[Object] In a case using a gallium nitride based compound semiconductor for a substrate, which necessitates polishing for flattening the surface of the gallium nitride based compound semiconductor substrate, the surface of the gallium nitride based compound semiconductor substrate receives physical damages and light emitted from a light emitting layer formed thereon is non-uniform. The object is to improve uniformity of emitted light by solving these problems.

[Means for Attaining the Object] A first n-type layer 13 containing at least In and a light emitting layer 15 are formed on a substrate made of a gallium nitride based compound semiconductor, wherein the first n-type layer 13 is formed between the substrate 11 and the light emitting layer 15 to improve uniformity of emitted light.

[Selected drawing] FIG. 2